SPECIFICATION

Damascene Interconnection and Semiconductor Device

TECHNICAL FIELD

This invention relates to damascene interconnections and semiconductor devices. More particularly, the invention relates to a damascene interconnection having a bonding pad formed by a pad trench and a metal or conductive film filling the pad trench, and to a semiconductor device using same.

PRIOR ART

Recently, so-called the damascene process has being adopted in providing multilevel interconnections for a semiconductor device having a metal or conductive film buried in the insulating film.

Briefly explaining a general damascene interconnection, an insulating film 2 formed on a semiconductor substrate 1 as shown in Figure 1(a) is etched using a mask of resist 3 patterned corresponding to an interconnection, as shown in Figure 1(b), thereby forming a trench 4. After removing away the resist 3, a conductive film 5 is formed covering the trench 4 as shown in Figure 1(c). Then, the conductive film 5 in areas other than the trench 4 is removed in a polishing process using, for example, a Chemical Mechanical Polish process (hereinafter referred to as "CMP process"), as shown in Figure 1(d).

It is known that, where removing the conductive film 5 by the CMP process, the greater is the opening area of the trench the higher is the polish rate on the conductive film buried in the trench, as shown in Figure 2. There encounters no especial problem in regions having a small trench opening area, such as in usual interconnections. However,

in regions having a large trench opening area, such as a bonding pad 6 shown in Figure 3, the conductive film 5 in the trench is polished into a dish-like form by an abrasive as shown in Figure 4, thus resulting in so-called dishing. Due to this, there are cases that disconnection or increase of resistance occurs in a central portion A where the wall thickness is reduced when providing connection between the bonding pad and the IC frame.

SUMMARY OF THE INVENTION

Therefore, it is a primary object of the present invention to provide a novel damascene interconnection and semiconductor device.

Another object of the invention is to provide a damascene interconnection capable of preventing resistance value increase or disconnection caused by dishing in a bonding pad, and a semiconductor device using the same.

A damascene interconnection according to the present invention, comprises: an interconnection trench formed in an insulating film and a pad trench communicating therewith; a protrusion formed by a portion not removed of the insulating film in the pad trench to decrease a substantial opening area of the pad trench; and a conductive film buried in the interconnection trench and the pad trench.

In the case of using such a damascene interconnection for a semiconductor device, such a semiconductor device, comprises: a semiconductor substrate; an insulating film formed on the semiconductor substrate; an interconnection trench formed on the insulating film and communicating with a semiconductor element; a pad trench formed on the insulating film and communicating with the interconnection trench; a protrusion formed by a portion of not removed of the insulating film in the pad trench and reducing a substantial opening area of the pad trench; and a conductive film buried in the

interconnection trench and the pad trench.

When removing the conductive film by a CMP process or the like, the protrusion dividing the pad trench serves as a stop of polishing by an abrasive. Consequently, so-called dishing will not occur that the conductive film in the pad trench is excessively removed. Thus, according to the invention, it is possible to prevent a bonding pad from being increased of resistance or causing disconnection resulting from dishing.

The protrusion may be formed not to divide the conductive film buried in the pad trench, or formed to divide the conductive film. However, where the conductive film is divided, another means is required to electrically couple together divided conductive film portions. The other means may be a contact hole for connecting between the conductive film formed in the insulating film and a conductive film arranged in a level lower than the insulating film. It should be noted that the contact hole is effective also where the conductive film in the pad trench is not divided by a protrusion.

The protrusion includes, in one embodiment, island protrusions distributed in a proper interval in the pad trench, and in another embodiment ridges.

The above described objects and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is an illustrative view showing a process for a general damascene interconnection;

Figure 2 is a graph showing a usual polish characteristic in CMP;

Figure 3 is an illustrative view showing a prior art;

Figure 4 is a sectional view on line IV-IV in Figure 3;

Figure 5 is an illustrative view showing one embodiment of the present invention;

Figure 6 is a sectional view on line VI-VI in Figure 5;

Figure 7 is an illustrative view showing a method for forming the Figure 5 embodiment;

Figure 8 is an illustrative view showing another embodiment of the invention;

Figure 9 is an illustrative view showing another embodiment of the invention;

Figure 10 is an illustrative view showing another embodiment of the invention;

Figure 11 is a sectional view on line - in Figure 10;

Figure 12 is an illustrative view showing another embodiment of the invention; and

Figure 13 is an illustrative view showing another embodiment of the invention.

BEST FORM FOR PRACTICING THE INVENTION

A semiconductor device 10 of this embodiment shown in Figure 5 and Figure 6 includes a semiconductor substrate 12 formed, for example, of silicon (Si) or the like. Note that the semiconductor substrate 12 may use any of other materials. Semiconductor elements, including active and/or passive elements, are formed on the semiconductor substrate 12, although they are not shown in the figure.

The semiconductor device 10 comprises a damascene interconnection 11 including, on the semiconductor substrate 12, an interconnection trench 16 extending from the semiconductor element (not shown) and a pad trench 18 connected to the interconnection trench 16. That is, an insulating film 14 is formed, for example, of silicon oxide (SiO_2) in a uniform film thickness on the semiconductor substrate. In the insulating film 14, the interconnection trench 16 and the pad trench 18 connected therewith are formed. The insulating film 14 may use any of other materials.

Note that Figure 5 and Figure 6 illustrate the insulating film 14 formed directly on the surface of the semiconductor substrate 12 in order for simplifying illustration and explanation. However, in the actual semiconductor device, one or a plurality of semiconductor element layers are formed on the semiconductor substrate 12 as well known in the art and an interconnection layers is formed as required on each of such semiconductor element layers. The interconnection trench 16 provides electrical connection between the semiconductor element (not shown) and the pad trench 18. The pad trench 18 serves as a bonding pad on which wire-bonding is to be made to a not-shown IC leadframe. That is, the pad trench 18 is a connection terminal to provide electric conduction of the semiconductor element on each layer to and from the IC leadframe.

It has been a conventional practice to form such a damascene interconnection 11 by merely filling a conductive film, such as of copper (Cu), aluminum (Al) or tungsten (W), in the interconnection trench 16 and pad trench 18.

In this embodiment, however, the following devising is implemented on the pad trench 18 comparatively large in opening area, in order to prevent against dishing as stated before. That is, the pad trench 18 has an insulating film 14 formed to be left as an island-spotted form. Consequently, the pad trench 18 is divided into unitary portions by island protrusions 20. However, the island protrusions 20 do not separate one portion from another portion of the pad trench 18, i.e. the pad trench 18 is continuous in areas except for the island protrusions 20. That is, the pad trench 18 in this embodiment has a large opening size but is reduced in substantial opening area by the presence of the island protrusions 20. Specifically, in this embodiment the pad trench 18 has a side determined as approximately 50 - 200 μm and an interval of the protrusions 20 determined as approximately 5 - 20 μm.

In the pad trench 18 thus having the island-spotted protrusions 20, a conductive film 22 is formed using a metal as mentioned before or conductive material in a manner similar to that of the interconnection trench 16. Thus, the semiconductor element (not shown) on the semiconductor device 10 is electrically coupled through the conductive film 22 buried in the interconnection trench 16 to the pad trench 18, i.e. the conductive film 22 buried in the pad trench 18. Due to this, by bonding a wire (not shown) to the conductive film 22 formed in the pad trench 18, the semiconductor element is put in electrical connection to the wire, i.e. to the IC leadframe.

Hereunder, explanation is made on a method to concretely manufacture a semiconductor device 10 of the embodiment having a damascene interconnection 11 as described above, with reference to Figure 7. Incidentally, in Figure 7 an insulating film 14 is formed directly on a surface of a semiconductor substrate 12. It should however be noted that the semiconductor device 10 in practical has a proper number of semiconductor element layers as stated before and Figure 7 depicts an interconnection structure having only one layer for the sake of convenience.

An insulating layer 14 is formed on a semiconductor substrate 12 by thermal oxidation process or the like, as shown in Fig. 7(a). Thereafter, the insulating film 14 is masked with patterned resist 24 to leave island protrusions 20. Etching is made to form an interconnection trench 16 and a pad trench 18. At this time, a plurality of island protrusions 20 are formed in the pad trench 18. After removing the resist 24, a conductive film 22 is formed over an entire surface of the semiconductor substrate 12 including the interconnection trench 16 and pad trench 18 by a CVD or hot sputter process, as shown in Fig. 7(c). Then, the conductive film 22 on the insulating film 14 is removed as shown in Fig. 7(d) by a CMP process.

In the CMP process, the semiconductor substrate 12 (including the insulating film

14 and the conductive film 22) is urged onto a polishing pad mounted on a polisher table. The table and the substrate holder are relatively rotated while supplying to the polishing pad a slurry containing abrasive particles. When the conductive film 22 on the insulating film 14 is removed, the polishing operation is finished. In this case, the abrasive particle for polishing is selected of kind (material, particle size, etc.) such that in CMP a polish rate on the insulating film 14 is lower than a polish rate on the conductive film 22. According to an experiment conducted by the present inventors, the polish rate in concrete is desirably given as (polish rate on the conductive film 22) / (polish rate on the insulating film 14) $\geqq$ 20 to 10. This is because in CMP the conductive film 22 on the insulating film 14 needs to be removed as rapid as possible. However, the insulating film 14 should be prevented from being damaged due to polishing, and the island projections 20 are to prevent over-polish to the conductive film 22 of the pad trench 18. Consequently, there is a necessity of providing the insulating film 14 with greater polish resistance than that of the conductive film 22.

According to this embodiment, in the process of removing the conductive film 22 (Figure 7(d)), the protrusions 20 (insulating film 14) having a low polish rate acts such that the conductive film 22 is decelerated in proceeding of polishing by the polish pad. Thus, the conductive film 22 in the pad trench 18 can be prevented from being removed to an excessive extent. This in turn makes it possible to prevent the pad trench 18 from increasing in resistance or occurrence of disconnection due to dishing.

That is, in the conventional art shown in Figure 3 and Figure 4, because the pad trench 6 is contacted in its entire opening by a polish pad (not shown), the pad trench 6 having a large opening area is partly over-polished into a result of dishing. On the contrary, in this embodiment, despite the pad trench entirely is large in opening area, the opening is divided into unitary portions wherein the opening area is small if considered

on a portion sandwiched between the island protrusions 20. Due to this, over-polish will not occur. As a result, a conductive film 22 in the pad trench 18 is given a planar surface as shown in Figure 6 and Figure 7(d).

In this manner, in the present invention, where using a CMP method having a polish characteristic that the polish rate increases with increase in opening area, the forming of protrusions in the pad trench reduces the substantial opening area thereby preventing dishing.

Incidentally, the protrusions 20 may be in a form to divide the pad trench 18 into portions. The shape of a protrusion may be a straight line as shown in Figure 8 or a squared-spiral form as shown in Figure 9.

That is, in the embodiment shown in Figure 8, a plurality of protrusions or ridges 20 are formed extending from respective outer edges of four sides of a rectangular pad trench 18. It should be noted that, in also this case, the other areas of the pad trench 18 are continuous with one another. In also this embodiment, the substantial opening area is reduced in the areas of between the protruding ridges 20, between protruding ridges extending from different sides and between the protruding ridge 20 and the inner edge of the pad trench 18.

In the embodiment of Figure 9, a pad trench 18 has one ridge 20 formed in a squared-spiral form. In the Figure 9 embodiment, because the ridge 20 is in the spiral form, the pad trench 18 is not divided into. In this manner, by forming the ridge 20 in the spiral form, the opening area is substantially reduced in the areas of between portions of the ridge 20 and between the ridge 20 and the pad trench 18 inner edge.

Meanwhile, if necessary, connection holes or contact holes 26 may be formed through a bottom of the pad trench 18 to provide electrical connection between the conductive film 22 and a not-shown lower-level conductive film through these contact

holes 26.

Explanation is made in detail on an embodiment having contact holes 26 formed through the insulating film 14, with reference to Figure 10 and Figure 11,. This embodiment is to be applied to a semiconductor device having another layer formed in a level lower the insulating film 14, as shown in Fig. 11. That is, another insulating film 28 is formed on a semiconductor substrate 12, and further another conductive film 30 is formed on the insulating film 28. The insulating film 14 is formed on the conductive film 30. In a bottom of the pad trench 18, a plurality of contact holes 26 are formed penetrating through the insulating film 14. When forming a metal or conductive film 22 in the pad trench 18, a metal or conductive material thereof is also filled in the contact holes 26 to provide electrical connection between the upper-leveled conductive film 22 and lower-leveled conductive film 30. By thus forming the contact holes 26 in the pad trench 18 and connecting between the conductive films 22 and 30, it is possible to eliminate the disadvantage as feared upon forming protrusions 20 in the pad trench 18.

That is, the protrusions or ridges if formed in the pad trench 18 results in volume decrease of the pad trench 18, i.e. volume reduction of the conductive film 22 of the pad trench 18. It is to be feared that the bonding pad be increased in electric resistance by volume reduction in the conductive film 22 of the pad trench 18. However, the conductive film 22 if coupled to the conductive film 30 as in the Figure 10 and Figure 11 embodiments increases the effective volume of the conductive film 22, thus properly suppressing the electric resistance from increasing.

In an embodiment shown in Figure 12, contact holes 26 are added to the structure of the Figure 8 embodiment to thereby make the conductive film 22 of the pad trench 18 integral with a lower-leveled conductive film.

In an embodiment of Figure 13, a ridge 20 is formed in a closed-loop form in a

manner different from the Figure 9 embodiment. Accordingly, in this embodiment the conductive film 22 of the pad trench 18 is divided into portions, in a manner different from the above embodiment. In this case, the contact holes 26 are especially effective. That is, the formation of contact holes 26 connects the conductive film 22 of the pad trench 18 to a lower-leveled conductive film 30 (Figure 11). Consequently, the divided portions of the conductive film 22 of the pad trench 18 are electrically coupled together through the conductive film 30. That is, in the Figure 13 embodiment, the ridge or protrusion 20 is formed in a closed-loop form. However, there encounters no problem with disconnection in the pad trench 18 due to the protrusion or ridge 20 because the conductive film 22 is coupled to the lower-leveled conductive film through the via holes 26.

Incidentally, in the present invention, the protrusion or ridge for reducing the actual opening area of the pad trench may be provided in plurality in the pad trench or employed one in number.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.